PATENT
5957-04501

POWER OF ATTORNEY; NOTICE OF CHANGE OF ADDRESS

Commissioner for Patents
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CHANGE OF ADDRESS

Applicant respectfully requests the Commissioner to change the correspondence address for any and all patent applications and patents filed by FAUST COMMUNICATIONS LLC.

Applicant's new correspondence address is:

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If there are any questions regarding this matter, please contact B. Noël Kivlin at the telephone number provided.

By: _____
Julia Ceffalo
Title: AUTHORIZED PERSON
Date: 11 JUL 2005

Exhibit B

ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, **NeoMagic Corporation** having offices at 3250 Jay Street, Santa Clara, CA 95054 ("***Assignor***"), does hereby sell, assign, transfer and convey unto Faust Communications, LLC, with an office at 3225 McLeod Dr., Ste. 100, Las Vegas, NV 89121 ("***Assignee***") or its designees, all of Assignor's right, title and interest in and to the patent applications and patents listed below, any patents, registrations, or certificates of invention issuing on any patent applications listed below, the inventions disclosed in any of the foregoing, any and all counterpart United States, international and foreign patents, applications and certificates of invention based upon or covering any portion of the foregoing, and all reissues, re-examinations, divisionals, renewals, extensions, provisionals, continuations and continuations-in-part of any of the foregoing (collectively "***Patent Rights***"):

Patent or Application No.	**Country**	**Filing Date**	**Title and Inventor(s)**
US5506499	US	June 5, 1995	Multiple probing of an auxiliary test pad which allows for reliable bonding to a primary bonding pad Puar; Deepraj S.
US5587672	US	September 25, 1995	Dynamic logic having power-down mode with periodic clock refresh for a low-power graphics controller Ranganathan; Ravi|Puar; Deepraj S.
US5615376	US	August 3, 1994	Clock management for power reduction in a video display sub-system Ranganathan; Ravi
US5754170	US	January 16, 1996	Transparent blocking of CRT re-fresh fetches during video overlay using dummy fetches Ranganathan; Ravi
US5757338	US	August 21, 1996	EMI reduction for a flat-panel display controller using horizontal-line based spread spectrum

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			Bassetti; Chester F.|Pimpalkhare; Mangesh S.|Dharmarajan; Krishnan C.
US5764201	US	April 22, 1996	Multiplexed yuv-movie pixel path for driving dual displays Ranganathan; Ravi
US5781200	US	August 8, 1996	Tile memory mapping for increased throughput in a dual bank access DRAM Lu; Hsuehchung Shelton|Fan; Huei-Yi
US5790083	US	April 10, 1996	Programmable burst of line-clock pulses during vertical retrace to reduce flicker and charge build-up on passive LCD display panels during simultaneous LCD and CRT display Bassetti; Chester F.
US5805126	US	May 8, 1996	Display system with highly linear, flicker-free gray scales using high framecounts Bassetti; Chester F.
US5877780	US	August 8, 1996	Semiconductor chip having multiple independent memory sections, at least one of which includes simultaneously accessible arrays Lu; Hsuehchung Shelton|Rossman; Andrew|LeNgoc; Dahn
US5900887	US	May 5, 1997	Multiplexed wide interface to SGRAM on a graphics controller for complex-pattern fills without color and mask registers Leung; Clement K.|Ranganathan; Ravi

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US5903480	US	September 29, 1997	Division-free phase-shift for digital-audio special effects Lin; Tao
US5907295	US	August 4, 1997	Audio sample-rate conversion using a linear-interpolation stage with a multi-tap low-pass filter requiring reduced coefficient storage Lin; Ta
US5929924	US	March 10, 1997	Portable PC simultaneously displaying on a flat-panel display and on an external NTSC/PAL TV using line buffer with variable horizontal-line rate during vertical blanking period Chen; Andy His-Wen
US5936683	US	September 29, 1997	YUV-to-RGB conversion without multiplies using look-up tables and pre-clipping Lin; Tao
US5943382	US	December 15, 1997	Dual-loop spread-spectrum clock generator with master PLL and slave voltage-modulation-locked loop Li; Hung-Sung|Pimpalkhare; Mangesh S.
US5970110	US	January 9, 1998	Precise, low-jitter fractional divider using counter of rotating clock phases Li; Hung-Sung
US6007228	US	May 21, 1997	Master digital mixer with digital-audio links to external audio in a docking station and to internal audio inside a portable PC Agarwal; Suresh|Dharmarajan;

			Krishnan C.
US6016151	US	September 12, 1997	3D triangle rendering by texture hardware and color software using simultaneous triangle-walking and interpolation for parallel operation Lin; Tao
US6023745	US	August 8, 1996	Scoreboarding for DRAM access within a multi-array DRAM device using simultaneous activate and read/write accesses Lu; Hsuehchung Shelton
US6043801	US	October 28, 1997	Display system with highly linear, flicker-free gray scales using high framecounts Bassetti; Chester F.
US6046735	US	April 6, 1998	EMI reduction for a flat-panel display controller using horizontal-line-based spread spectrum Bassetti; Chester F.|Pimpalkhare; Mangesh S.|Dharmarajan; Krishnan C.
US6049316	US	June 12, 1997	PC with multiple video-display refresh-rate configurations using active and default registers Nolan; Rebecca|Tang; Richard X.
US6057789	US	October 29, 1998	Re-synchronization of independently-clocked audio streams by dynamically switching among 3 ratios for sampling-rate-conversion Lin; Tao
US6057809	US	May 20, 1998	Modulation of line-select times of individual rows of a flat-panel display for gray-scaling Singhal; Dave M.|Bassetti; Chester F.

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US6072415	US	October 29, 1998	Multi-mode 8/9-bit DAC with variable input-precision and output range for VGA and NTSC outputs Cheng; Yu-Chi
US6078513	US	August 16, 1999	NMOS dynamic content-addressable-memory CAM cell with self-booting pass transistors and local row and column select Ong; Adrian E.|Puar; Deepraj S.
US6091386	US	June 23, 1998	Extended frame-rate acceleration with gray-scaling for multi-virtual-segment flat-panel displays Lin; Tao
US6101620	US	July 18, 1997	Testable interleaved dual-DRAM architecture for a video memory controller with split internal/external memory Ranganathan; Ravi
US6104658	US	September 29, 1998	Distributed DRAM refreshing Lu; Hsuehchung Shelton
US6157978	US	January 6, 1999	Multimedia round-robin arbitration with phantom slots for super-priority real-time agent Ng; David Way|Mathur; Harish Narian
US6184894	US	January 29, 1999	Adaptive tri-linear interpolation for use when switching to a new level-of-detail map Rosman; Andrew|Pimpalkhare; Mangesh S.
US6188411	US	July 2, 1998	Closed-loop reading of index registers using wide read and narrow write for multi-threaded system

			Lal; Michael Man Lok
US6188594	US	June 9, 1999	Reduced-pitch 6-transistor NMOS content-addressable-memory cell Ong; Adrian E.
US6189082	US	January 29, 1999	Burst access of registers at non-consecutive addresses using a mapping control word Ramamurthy; Sriram
US6205524	US	September 16, 1998	Multimedia arbiter and method using fixed round-robin slots for real-time agents and a timed priority slot for non-real-time agents Ng; David Way
US6222550	US	December 17, 1998	Multiple triangle pixel-pipelines with span-range pixel interlock for processing separate non-overlapping triangles for super-scalar 3D graphics engine Rosman; Andrew|Li; Ming-Ju
US6230235	US	September 29, 1998	Address lookup DRAM aging Lu; Hsuehchung Shelton|Keene; David
US6236347	US	March 31, 2000	Dual-mode graphics DAC with variable 8/9-bit input-precision for VGA and NTSC outputs Cheng; Yu-Chi
US6252919	US	December 17, 1998	Re-synchronization of independently-clocked audio streams by fading-in with a fractional sample over multiple periods for sample-rate conversion Lin; Tao
US6260054	US	October 29, 1998	Reciprocal generator using piece-wise-linear segments of varying

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			width with floating-point format Rosman; Andrew|Lin; Tao
US6272283	US	April 22, 1998	Copy-protection for laptop PC by disabling TV-out while viewing protected video on PC display Nguyen; Thu N.
US6295068	US	April 6, 1999	Advanced graphics port (AGP) display driver with restricted execute mode for transparently transferring textures to a local texture cache Peddada; Vijay|Ranade; Shreekant M.
US6308220	US	January 29, 1999	Circulating parallel-search engine with random inputs for network routing table stored in a wide embedded DRAM Mathur; Harish N.
US6374148	US	October 13, 1999	Portable-PC audio system with digital-audio links to external audio in a docking station Dharmarajan; Krishnan C.|Agarwal; Suresh
US6421466	US	September 29, 1999	Hierarchical motion estimation with levels of varying bit width for digital video compression Lin; Tao
US6424658	US	February 17, 1999	Store-and-forward network switch using an embedded DRAM Mathur; Harish N.
US6433789	US	February 18, 2000	Steaming prefetching texture cache for level of detail maps in a 3D-graphics engine Rosman; Andrew

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US6473529	US	November 3, 1999	Sum-of-absolute-difference calculator for motion estimation using inversion and carry compensation with full and half-adders Lin; Tao
US6501482	US	October 11, 2000	Texture map blender with adaptive interpolation when switching to a new level-of-detail map Rosman; Andrew|Pimpalkhare; Mangesh S.
US6564329	US	March 16, 1999	System and method for dynamic clock generation Cheung; Edmund|Sponring; Otto
US6591286	US	January 18, 2002	Pipelined carry-lookahead generation for a fast incrementer Lu; Wei-Ping
US6628330	US	November 3, 1999	Color interpolator and horizontal/vertical edge enhancer using two line buffer and alternating even/odd filters for digital camera Lin; Tao
US6642962	US	September 1, 1999	Merged pipeline for color interpolation and edge enhancement of digital images Lin; Tao|Yu; Vincent Chor-Fung|Tang; Tianhua|Hwang; Beong-Kwon
US6680738	US	February 22, 2002	Single-block virtual frame buffer translated to multiple physical blocks for multi-block display refresh generator Ishii; Takatoshi|Cheung; Edmund|Brannon; Sherwood
US6721000	US	February 23, 2000	Adaptive pixel-level color enhancement for a digital camera

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			Lin; Tao|Tang; Tianhua
US6741257	US	January 20, 2003	Graphics engine command FIFO for programming multiple registers using a mapping index with register offsets Retika; John Y.
US6791576	US	February 23, 2000	Gamma correction using double mapping with ratiometrically-related segments of two different ratios Lin; Tao

Assignor further agrees to and hereby does sell, assign, transfer and convey unto Assignee all rights: (i) in and to causes of action and enforcement rights for the Patent Rights including all rights to pursue damages, injunctive relief and other remedies for past and future infringement of the Patent Rights, and (ii) to apply in any or all countries of the world for patents, certificates of invention or other governmental grants for the Patent Rights, including without limitation under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement or understanding. Assignor also hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents or certificates of invention which may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

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IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Santa Clara, CA on April 6, 2005.

ASSIGNOR

By: Scott Sullinger

Name: Scott Sullinger

Title: CFO

CALIFORNIA ALL-PURPOSE ACKNOWLEDGMENT

STATE OF CALIFORNIA
COUNTY OF SANTA CLARA ss.

On this 6 of APRIL 2005 ,before me, WILLIAM F.BRONNER Notary Public,

Personally appeared SCOTT SULLINGER

☐ personally known to me or ☒ proved to me on the basis of satisfactory evidence to be the person/s whose name /s is/are subscribed to the within instrument and acknowledged to me that he/~~she/they~~ executed the same in his/her/their authorized capacity/ies, and that by his/~~her/their~~ signature/s on the instrument the person /s or the entity upon behalf of which the person /s acted, executed the instrument.
WITNESS my hand and official seal.

Signature William F Bronner

WILLIAM F. BRONNER
COMM. NO. 1378031
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